## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Stephan Voges et al.

Application No. : 09/521,280

Filed : 07 March 2000

For : Methods and Apparatus for Hardware Simulation and

Design Verification

Group Art Unit : 2192

Examiner : ERIC B. KISS

Mail Stop AF Commissioner for Patents P.O. BOX 1450 Alexandria, VA 22313-1450

## **REPLY TO FINAL OFFICE ACTION**

Sir:

Applicants reply to the 19 May 2006 Final Office Action. Please amend the application as follows: